Characteristic Description

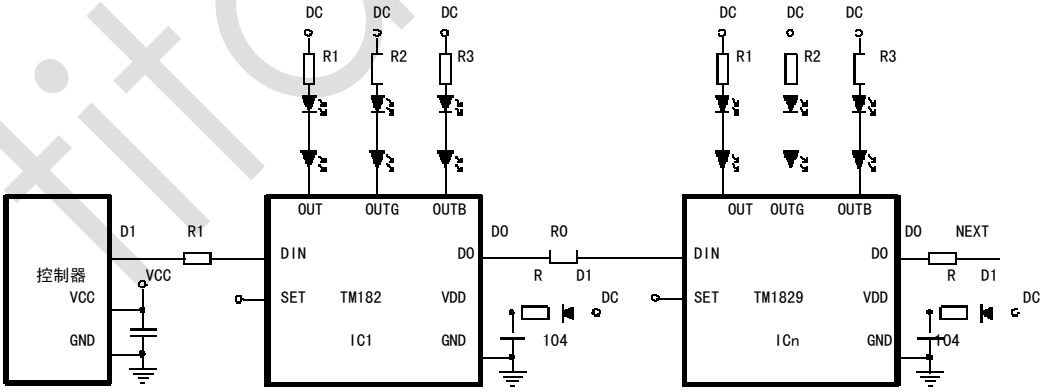
TM1829, inside which the MCU single-line digital interface, data latch, LED constant-current drive etc circuits and PWM luminance control circuit are integrated, is the circuit used specially by three-channel LED (Light-Emitting Diode) constant-current drive control. Chip can cascade through single-line digital interface (DI, DO).External controller can control the chip and the cascaded subsequent chip only through single line. The constant-current value of TM1829 output port and PWM luminance can be set separately through peripheral controller. 5V stabilivolt is integrated inside VDD pin. Peripheral component is few. The performance of the product is excellent with reliable quality.

Function Characteristics

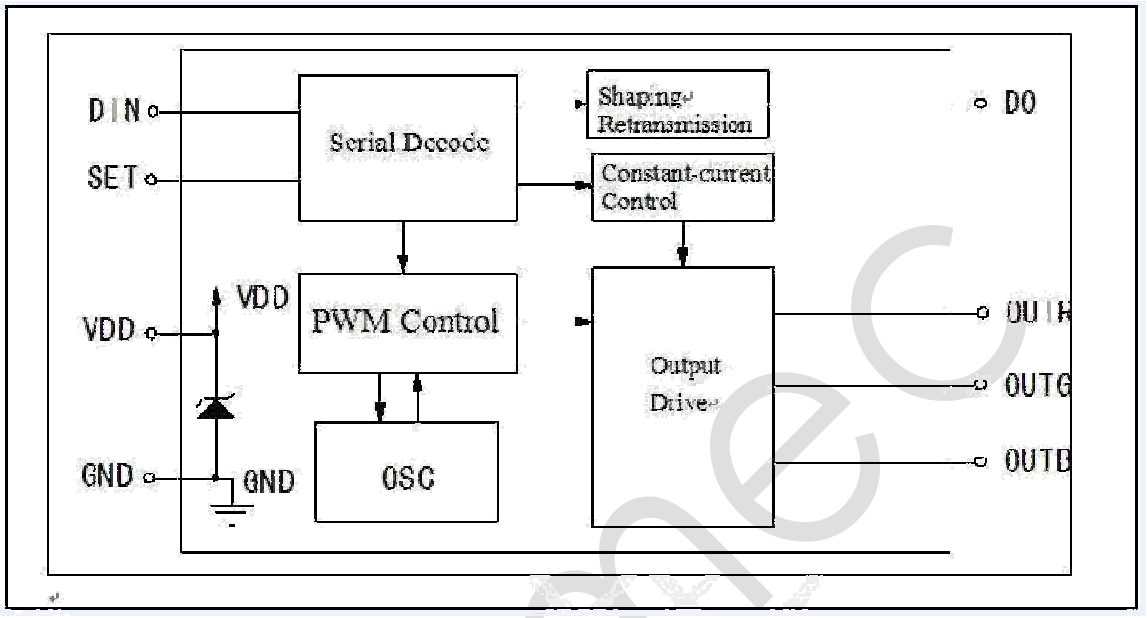
- Adopt power CMOS technology
- OUT output port can withstand voltage 24V
- VDD built-in 5V stabilivolt. Voltage supports 6～24V after resistance is connected in series.
- Luminance regulating circuit.256 level luminance is adjustable.
- Single-line serial interface.
- Oscillation mode：Built-in oscillation and have clock synchronization according to the signal in the data line. After receiving the data of the unit, it can send regenerated subsequent data automatically to lower level through the data output terminal, signal is not distorted or attenuated as cascade falls out.
- Built-in power-on reset circuit.
- PWM control terminal can realize 256 level regulation，scanning frequency 7KHZ
- Constant current can realize 32 level regulation（10mA—41mA）
- Can finish the receiving and decoding of data through one signal wire.
- When refresh rate is 30 frame/s hour，the number of cascade is not less than 1024 points under the low-speed mode and not less than 2048 points under high-speed mode.
- Data transmission rate can reach 800Kbps and 1.6Mbps two modes.
- Transmission distance between any two points is not less than 30 meters.
- Encapsulation mode：SOP8、DIP8

External Application Diagram

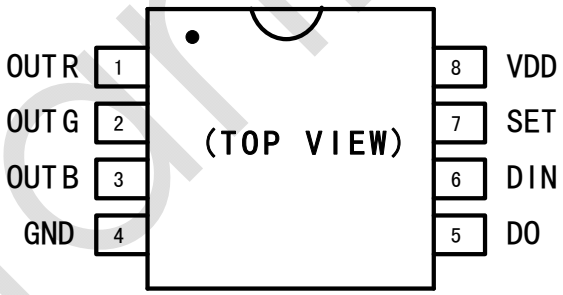
Application fields：Point light source, LED hurdle lamp, LED strip, indoor, outside big screen etc.



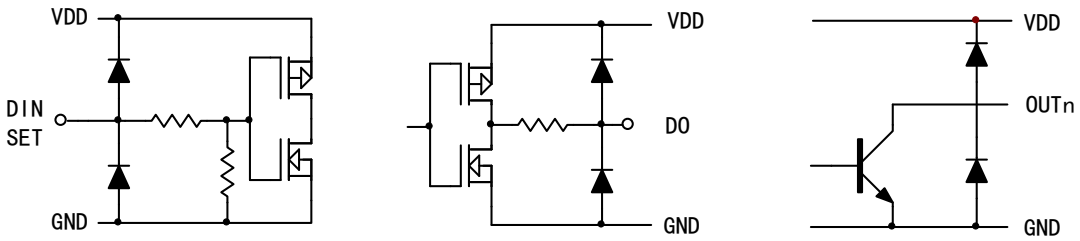
Internal Structure Diagram



Pin Information



Input and Output Equivalent Circuit



Pin Function

Port		I/O	Function Description
Name	Pin		
DIN	6	I	Data input
DO	5	O	Data output
SET	7	I	Connected with VDD: High-speed mode; Connected with GND or dangling |: Low-speed mode.
OUTR	1	O	Red PWM constant-current output.
OUTG	2	O	Green PWM constant-current output.
OUTB	3	O	Blue PWM constant-current output.
VDD	8	-	Logic power source
GND	4	-	Negative pole

A large amount of static electricity may be caused under dry season or dry working environment. Electrostatic discharge may damage integrated circuit. Titan Micro Electronics suggests adopting all proper integrated circuit preventive treatment measures. Improper operation and welding may cause the damage to ESD or lower its performance. Chip can not work normally.

Absolute Maximum Nominal Value Range (1)(2)

Parameter			Range	Unit
VDD	Logic power source voltage		-0.5～+7.0	V
VIN	Input terminal voltage range	DIN,SET	-0.5～VDD+0.7	V
IOUT	Output terminal current (DC)	OUTR,OUTG,OUTB	41	mA
VOUT	Output terminal voltage range	OUTR,OUTG,OUTB	-0.5～+30.0	V
FCLK	Clock frequency	DIN	2.0	MHZ
Topr	Working temperature range		-40～+85	℃
Tstg	Storage temperature range		-55～+150	℃
ESD	Human body mode（HBM）		4000	V
	Machine mode（MM）		400	V

（1）For these grades on the above table, chip used for a long time may cause the permanent damage to component to lower the reliability of component. We do not suggest that chip works by exceeding these limit parameters under other any conditions.

（2）All the voltage values are methodically tested.

Recommended working condition range

（Under -40℃~+85℃,GND=0V）unless otherwise specified.

Parameter		Test condition	TM1829			Unit
			Minimum value	Typical value	Maximum value	
DC parameter specification						
VDD	Power voltage		4.5	5.0	5.5	V
V_{DIN}	DIN input range of withstanding voltage	DIN series 1k resistance	-0.5	--	VDD+0.7	V
V_{SET}	SET input range of withstanding voltage	SET series 1K resistance	-0.5	--	VDD+0.7	V
V_{DO}	DO output range of withstanding voltage	DO series 1K resistance	-0.5	--	VDD+0.7	V
V_{OUT}	OUT output range of withstanding voltage	OUT = OFF	-0.5	--	24.0	V
TA	Working temperature range		-40		+85	℃
TJ	Working temperature range		-40		+125	℃

Electrical Characteristics

（Under VDD=5.0V and-40℃~+85℃，typical value VDD=5.0Vand TA=+25℃）unless otherwise specified.

Parameter		Test condition	TM1829			Unit
			Minimum value	Typical value	Maximum value	
VOH	High level output voltage	IOH=-6mA：DO	VDD-0.5	VDD	VDD+0.5	V
VOL	Low level output voltage	IOL=10mA：DO			0.4	V
VIH	High level input voltage	VDD=5.0V	3.5		VDD	V
VIL	Low level input voltage	VDD=5.0V	0		1.35	V
IOH	High level output current	VDD=5.0V,SDO=5.0V		1		mA
IOL	Low level output current	VDD=5.0V,SDO=1.0V		10		mA
IIN	Input current	DIN connected with VDD or GND	-1		1	uA
ICC0	Logic power source current（VDD）	OUTR,OUTG,OUTB ,DIN,SET,DO=open circuit	1.2	3.0	4.2	mA
IOLC	Constant output current range	OUTR,OUTG,OUTB=3.0V	10		41	mA
IOLKG	Output leakage current	OUTR, OUTG, OUTB =OFF	0		0.3	uA
T_{PWM}	OUT port duty ration period	OUT connected with resistance	135	140	145	us
ΔIOLC0	Constant-current error (Channel to channel）	OUTR, OUTG, OUTB =ON,VOUTn =1V			±3	%
ΔIOLC1	Constant-current error（Chip to chip）	OUTR, OUTG, OUTB =ON,VOUTn =1V			±6	%
ΔIOLC2	Linear regulation	OUTR, OUTG, OUTB =ON,VOUTn =1V		±0.5	±1	%/V
ΔIOLC3	Load regulation	OUTR, OUTG, OUTB =ON,VOUTn =1V~3V		±1	±3	%/V
IDDdyn	Dynamic current loss	OUTR, OUTG, OUTB =OFF DO=open			3	mA
Rth(j-a)	Thermal resistance		79.2		190	℃/W
PD	Consume power	(Ta=25°C)			250	mW

Switch Characteristics

（Under VDD=5.0Vand -40℃~+85℃，typical value VDD=5.0Vand TA=+25℃）unless otherwise specified.

Symbol	Parameter	Test condition	Minimum Value	Typical Value	Maximum Value	Unit
fosc1	Low-speed mode	DIN dangling or connect GND		800		KHz
fosc2	High-speed mode	DIN connect VDD		1.6		MHz
FOUT	OUT PWM output frequency	OUTR, OUTG, OUTB	6.5	7	7.5	KHZ
tPLZ	Transmission delay time	DIN → DOUT			200	ns
tPZL		CL = 15pF, RL = 10K Ω			100	ns
TTHZ	Fall time	CL = 300pF, OUTR/OUTG/OUTB			80	μs
CI	Input capacitance				15	pF

Function Description

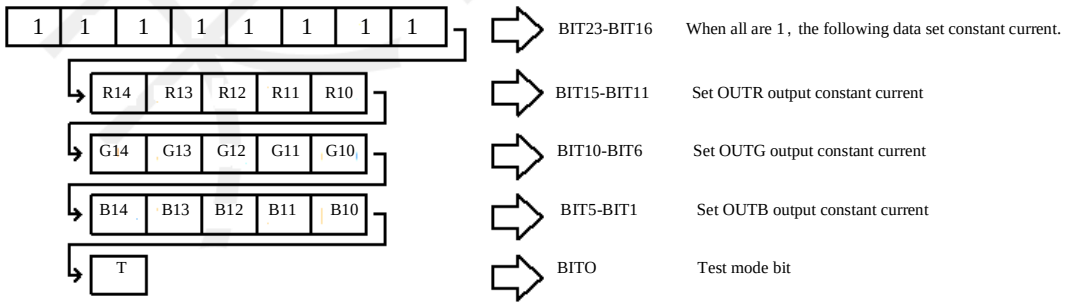
The single-line communication way and sending signal by adopting return-to-zero way are adopted by the chip. After the chip is power-on and reset, it receives the data sent by DIN terminal. After finishing receiving 24bit, DO port begins to retransmit the data sent by DIN terminal continuously to provide the input data for the next cascaded chip. Before retransmitting data, DO port is always high level. If DIN inputs RESET signal, chip will output corresponding PWM duty ration wave form according to the received 24bit data after resetting successfully and waits for receiving new data. After finishing receiving the original 24bit data, retransmit data through DO port. Before receiving RESET signal, OUTR, OUTG, OUTB pins original output keep unchanged.

Automatic waveshaping retransmission technology is adopted in chip. Signal will not be distorted and attenuated. The number of cascade of chip is not limited by the signal transmission and only limited by demand of scanning speed.

Data Structure

Constant-current mode command：

After chip is power-on and reset，data input by DIN is complete data packet after each continuous 24bit. Firstly send high byte，if high 8 bits [bit23~bit16] are 1 in full，and then the data packet is constant-current set data. The structure is as follows:



RI [bit15~bit11]:Set R channel constant-current value，Ir=10+RI[4:0]mA, namely minimum 10+0=10mA,maxium 10+31=41mA

GI [bit10~bit6]:Set G channel constant-current value. The setting method is the same as above.

BI [bit5~bit1]: Set B channel constant value. The setting method is the same as above.

T: Test mode bit. 1：When it is in this position，test mode

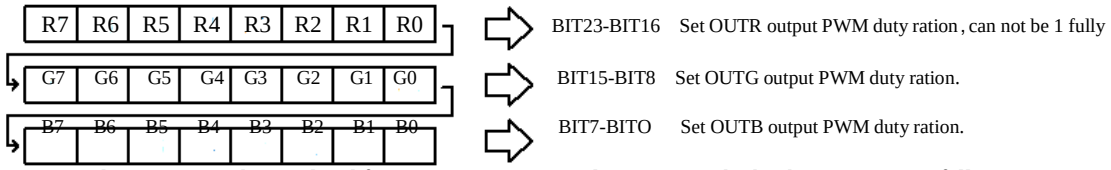
0：When this bit is reset，normal working mode，OUT outputs PWM

[bit15~bit1]bits are used to set OUTR，OUTG, OUTB pin output constant-current value independently. Numerical value range is from 0 to 31 and corresponds with the constant-current value in the following table.

OUTR	RI4	RI3	RI2	RI1	RI0	Numeric al value	Constant-current value（mA）
	BIT15	BIT14	BIT13	BIT12	BIT11		
OUTG	GI4	GI3	GI2	GI1	GI0		
	BIT10	BIT9	BIT8	BIT7	BIT6		
OUTB	BI4	BI3	BI2	BI1	BI0		
	BIT5	BIT4	BIT3	BIT2	BIT1		
	0	0	0	0	0	0	10
	0	0	0	0	1	1	11
	0	0	0	1	0	2	12
	0	0	0	1	1	3	13
	0	0	1	0	0	4	14
	0	0	1	0	1	5	15
	0	0	1	1	0	6	16
	0	0	1	1	1	7	17
	0	1	0	0	0	8	18
	0	1	0	0	1	9	19
	0	1	0	1	0	10	20
	0	1	0	1	1	11	21
	0	1	1	0	0	12	22
	0	1	1	0	1	13	23
	0	1	1	1	0	14	24
	0	1	1	1	1	15	25
	1	0	0	0	0	16	26
	1	0	0	0	1	17	27
	1	0	0	1	0	18	28
	1	0	0	1	1	19	29
	1	0	1	0	0	20	30
	1	0	1	0	1	21	31
	1	0	1	1	0	22	32
	1	0	1	1	1	23	33
	1	1	0	0	0	24	34
	1	1	0	0	1	25	35
	1	1	0	1	0	26	36
	1	1	0	1	1	27	37
	1	1	1	0	0	28	38
	1	1	1	0	1	29	39
	1	1	1	1	0	30	40
	1	1	1	1	1	31	41

PWM mode command:

If high 8 bits are not 1 in full in 24bit data packet, the data packet is PWM setting data. The structure is as follows:



PWM duty ration can be regulated from 0 to255 continuously. Attention: high 8 bits are not 1 in full.

The high bits are sent firstly when 24bit data is sent. It is sent according to the sequence of RGB 24 bits can be split into three 8 bits data to be sent. Be noted that the high level time between bytes can not exceed the RESET signal time, otherwise chip will be reset to receive data again, then data transmission can not be realized.

Low-speed mode time

Symbol	Parameter	Test condition	Minimum value	Typical value	Maximum value	Unit
T0L	Input 0 code, low level time	VDD=5V GND=0V	150	300	450	ns
T1L	Input 1 code, low level time		600	800	1000	ns
T0L'	Output 0 code, low level time		--	340	--	ns
T1L'	Output 1code, low level time		--	680	--	ns
T	0 code or 1 code cycle time		1200		--	ns
Treset	Reset code, high level time		140	500		us

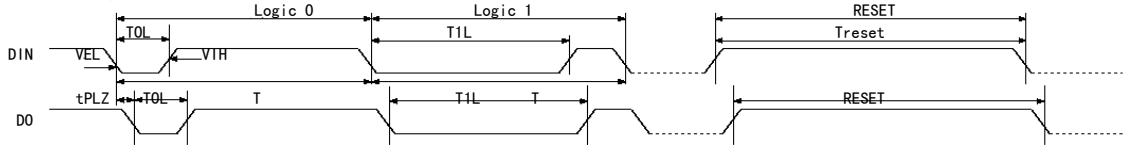
Note: The cycle time of sending1 code or 0 code under the low-speed mode is 1200ns (frequency 800KHZ).

High-speed mode time

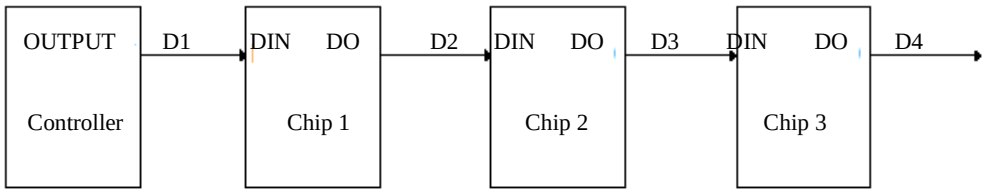
Symbol	Parameter	Test condition	Minimum value	Typical value	Maximum value	Unit
T0L	Input 0 code, low level time	VDD=5V GND=0V	50	170	250	ns
T1L	Input 1 code, low level time		300	450	550	ns
T0L'	Output 0 code, low level time		--	170	--	ns
T1L'	Output 1code, low level time		--	340	--	ns
T	0 code or 1 code cycle time		600		--	ns
Treset	Reset code, high level time		140	500		us

Note: The cycle time of sending 1 code or 0 code under high-speed mode is 600ns (frequency 1.6MHZ). Treset reset time of high-speed mode is the same.

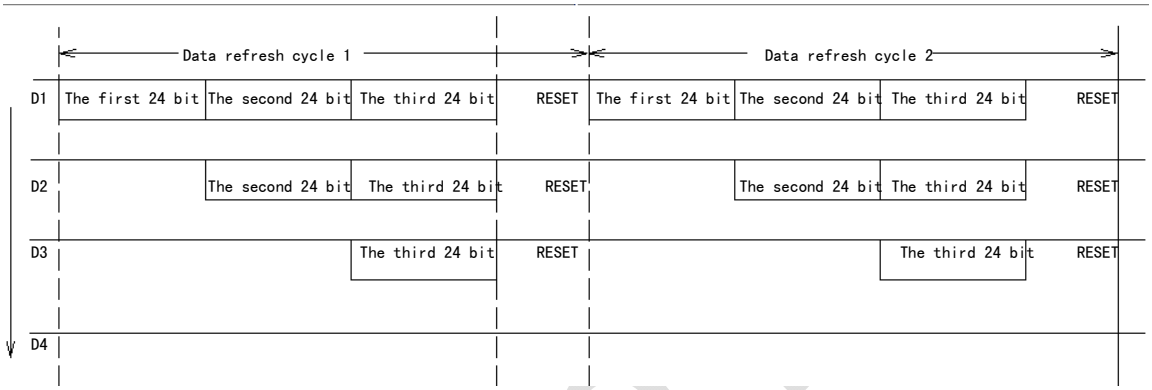
Time Sequential Diagram



Data Transmission and Retransmission



D1 is the datum transmitted by controller，D2,D3,D4 are the data retransmitted by cascade TM1829.



Chip cascade, data transmission and retransmission procedure: Data（D1）is sent from controller. When chip 1 finishes receiving the first 24bit, chip 1 does not retransmit data（D2）still and controller continues to send data, chip 1 receives the second 24bit. As the first 24 bit is existed in chip1, chip 1 retransmits the second 24bit out through DO. Chip 2 receives the data（D2）retransmitted from Chip1.At this time, chip 2 still does not retransmit data（D3）.Controller continues to send data. Chip 1 retransmits the received the third 24bit to chip 2.As one 24bit is existed in chip 2, chip 2 retransmits the third 24 bit（D3）Chip 3 receives the third 24bit. At this time, if controller sends one RESET high level signal, all chips will be reset and decodes the received 24 bit by its own respectively to control RGB port export to complete a data refresh cycle. Chip returns to the situation of preparing for receiving.

Application Information

1. How to calculate data refresh rate

Data refresh time is calculated according to quantity of cascade pixel point in one system. Generally one group of RGB is one pixel and needs to be controlled by one TM1829 chip.

Compute according to high-speed mode.

The highest transmission rate of BIT is 600ns（frequency1.6MHZ），One pixel datum includes red（8BIT），green（8BIT），blue（8BIT）total 24BIT.Transmission time is 24×0.6uS=14.4uS.If there are total 2000 pixel points in one system, the time displayed for refreshing all once is 14.4 uS×2000=28.8mS（ignore RESET code time，namely the refresh rate of one second is：1÷28.8×1000≈34.7Hz.

Scanning speed rate of low-speed mode reduces twice under corresponding high-speed mode.

This is the table of the corresponding highest data refresh rate of cascade dot matrix:

	High-speed mode		Low-speed mode	
Pixel	The quickest time of refreshing data (mS)	The highest refresh rate (Hz)	The quickest time of refreshing data (mS)	The highest refresh rate (Hz)
1~500	7.2	138	14.4	69
1~800	11.52	87	23.04	44
1~1000	14.4	69	28.8	35
1~1500	21.6	46	43.2	23
1~1800	25.92	38	51.84	19
1~2000	28.8	35	57.6	17

If system does not have high requirements on data refresh rate, then it will not have requirements on the quantity of cascade dot matrix. Only if power supply is normal, theoretically TM1829 unlimited cascade can be used.

2. How to make TM1829 work under optimum constant-current condition

TM1829 output is constant-current drive. It can be known when outputting according to constant-current curve. The voltage of OUT terminal needs to be over 1.2V for entering constant-current area when constant current is 41mA, then the chip has the constant-current effect. It doest not mean that the higher the voltage of the OUT terminal is, the better it is. The larger the power lost is on the chip, the more serious the release of the heat of chip is so that the reliability of the whole system is lowered. It is suggested that it is better that voltage Vout is controlled between 1.2~3V when OUT terminal is started. It is to be used by using series resistance way. Resistance theory compute mode is selected and used as follows:

System drive voltage: VDD

Single LED conducting voltage drop: Vled

The number of series LED: n

Constant-current value: Iout

Constant-current voltage: 1.5V

Resistance: R

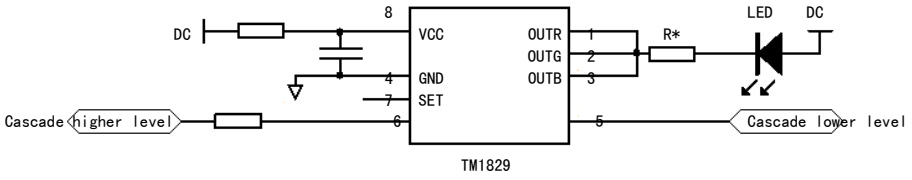
$$R=(VDD-1.5-n\times Vled)/ Iout$$

Example: System power supply 24V, single LED conducting voltage drop: 2V, The number of series LEDD: 6, constant-current value is 40mA

Resistance should be connected in series: R=(24-1.5-2×6)/0.04=262.5Ω , only around 260Ω resistance needs to be connected in series in the OUT pin.

3. Use TM1829 how to enlarge current

Each OUT port of TM1829 can only output 41mA constant current maximum. If user needs expand constant-current value drive, he can use after shorting three OUT ports. After shorting one OUT port, the maximum sum of constant-current will increase 41mA. The highest constant current can reach around 123mA after shorting three. The shortcoming of this method is that software is needed to cooperate to control at the same time to write three groups of register value separately. The advantage is that it can obtain the wanted current value with large constant current.



4. Power Configurations

TM1829 can be configured to DC6～24V voltage power supply, but different power resistance should be configured according to different input voltage. The method of calculating resistance: as the power will be lowered with the increase of load, the current flowing through VDD pin should be set to be calculated based on 4.5mA, the series VDD resistance R=（DC-5.0V）/4.5mA（DC is power voltage）.

The typical values of configured resistance are listed as follows:

Power Source Voltage DC	It is suggested that resistance is connected between power interface and VDD.
5V	No resistance needs to be connected，internal regulator does not work.
6V	100
9V	750
12V	1.5K
24V	3.9K

When SET terminal is in high level，it should be connected with VDD，External power source VCC is prohibited to be connected to prevent chip from break downing. It is suggested that blocking diode should be connected to protect chip.

5. The method of using program to drive LED

5.1 In order to realize the control of chip on LED luminance，firstly the voltage of RGB port should be ensured to make chip enter constant-current work（refer to Constant-current curve for details）;

5.2 Chip is power-on and reset. Initialize and set constant-current value firstly and the test mode bit T is 0（allow PWM to output）. If the constant current of output channel is set to be 20mA, the maximum current that is allowed to flow through is 20mA. The constant-current value should be set according to LED.

5.3 Write PWM register. Set PWM output. If the PWM luminance level of the RGB of output channel is set as 100, then current flowing through LED is 100÷256×20mA=7.8mA;

5.4 Keeping on changing PWM value，and then the LED luminance can be regulated arbitrarily. Set PWM value as 0，output are full high，and LED goes out. Set PWM value as FFH（Attention: 24BIT high 8 bits can not be 1 in full）and output maximum low level duty ration wave shape. LED is the brightest.

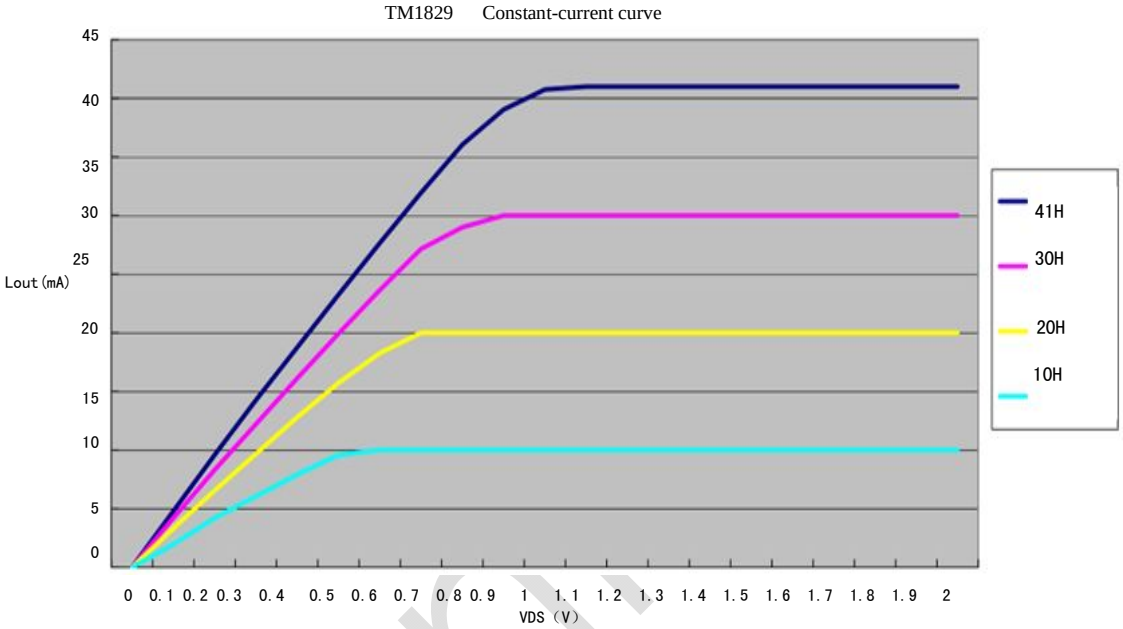
5.5 If setting constant-current value and test mode bit T is 1, then it enters test mode.

Notes：In order to avoid that the power of chip fails and is on and the power of controller does not fail to cause the set initialized constant-current register value to lose and the constant current change, it is suggested that the constant-current register should be refreshed regularly or the PWM register is refreshed once when the constant-current register is refreshed during the process of refreshing PWM register.

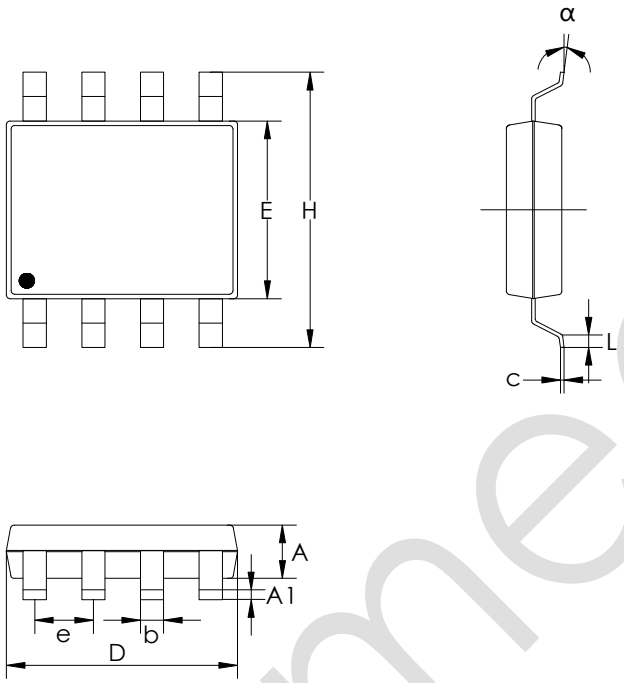
Constant-current Curve

When applying TM1829 to LED panel design, the current difference between channels and chips is minimum. This is from the outstanding characteristics of TM1829:

- When the voltage of load port changes, the stability of export current is not affected. Illustrated as follows:
- Shown as plot. The relationship of the current Iout with the voltage Vds on the port can be known. Under the constant-current working condition, port export Iout is constant-current value. The smaller the Iout constant current is, the smaller the needed Vds is. The minimum can not be less than 0.8V.
-

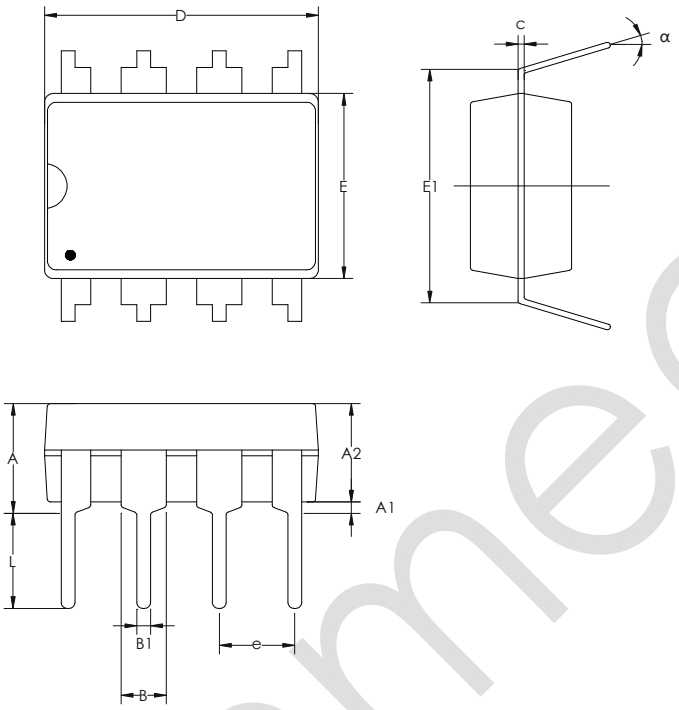


Encapsulation Diagram（SOP8）



	Inch			MM		
Symbol	**Minimum**	**Standard**	**Maximum**	**Minimum**	**Standard**	**Maximum**
A	0.051	0.059	0.067	1.30	1.50	1.70
A1	0.002	0.006	0.010	0.06	0.16	0.26
b	0.012	0.016	0.022	0.30	0.40	0.55
c	0.006	0.010	0.014	0.15	0.25	0.35
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.163	3.75	3.95	4.15
e		0.050			1.27	
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.018	0.026	0.033	0.45	0.65	0.85
α	0°		8°	0°		8°

Encapsulation Diagram（DIP8）



	Inch			MM		
Symbol	**Minimum**	**Standard**	**Maximum**	**Minimum**	**Standard**	**Maximum**
A			0.170			4.31
A1	0.015			0.38		
A2	0.124	0.134	0.144	3.15	3.4	3.65
B	0.015	0.018	0.020	0.38	0.46	0.51
B1	0.050	0.060	0.070	1.27	1.52	1.77
c	0.008	0.010	0.012	0.20	0.25	0.30
D	0.352	0.362	0.372	8.95	9.20	9.45
E	0.242	0.252	0.262	6.15	6.40	6.65
E1		0.300			7.62	
e		0.100			2.54	
L	0.118	0.130	0.142	3.00	3.30	3.60
α	0°		15°	0°		15°